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What is the LVDS ?

LVPECL ?

Prepared by r. k. shih on 2004/12/8
E-mail : r_k_shih@aker.com.tw

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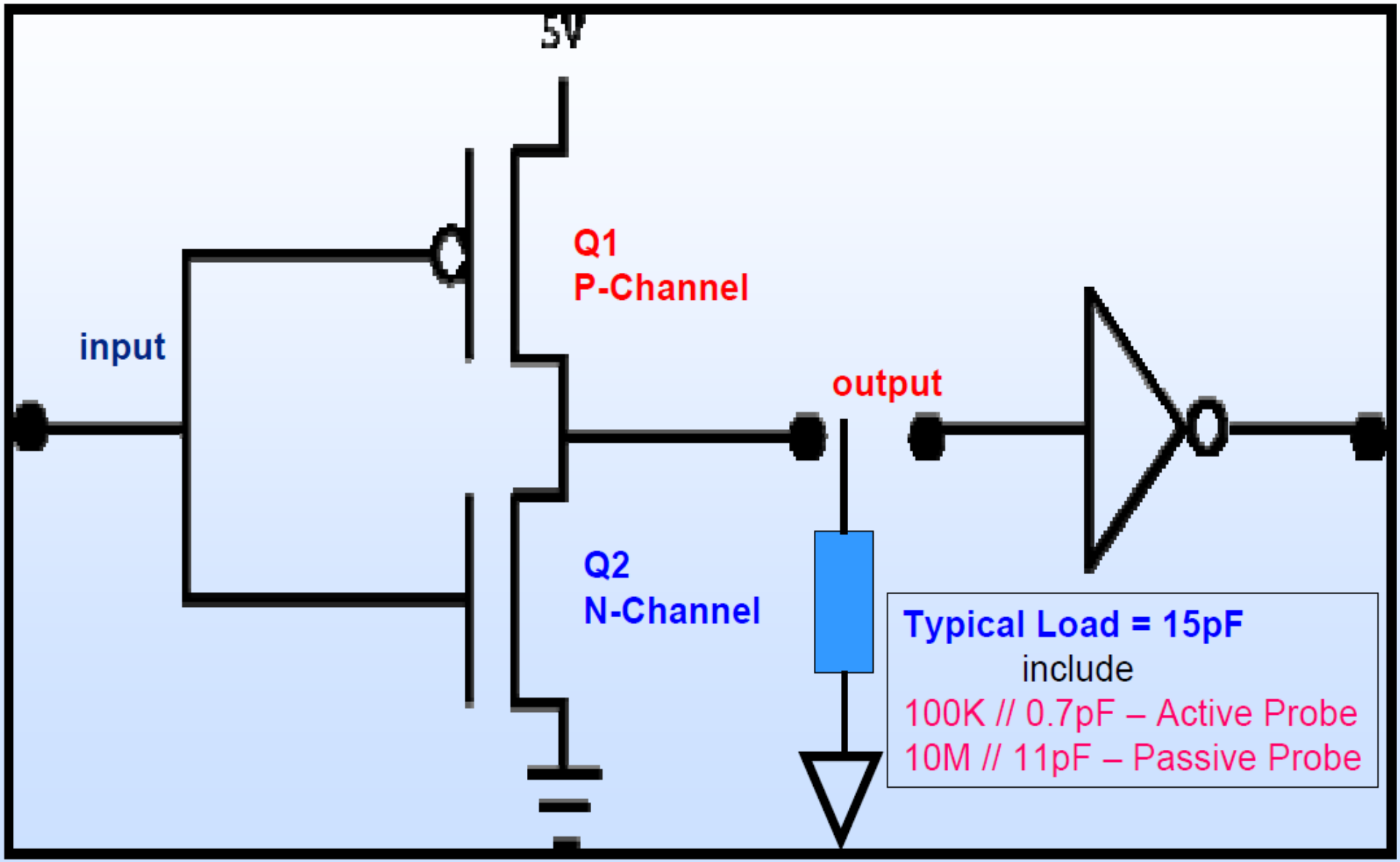
CMOS output LOGIC



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LVPECL/LVDS output circuit

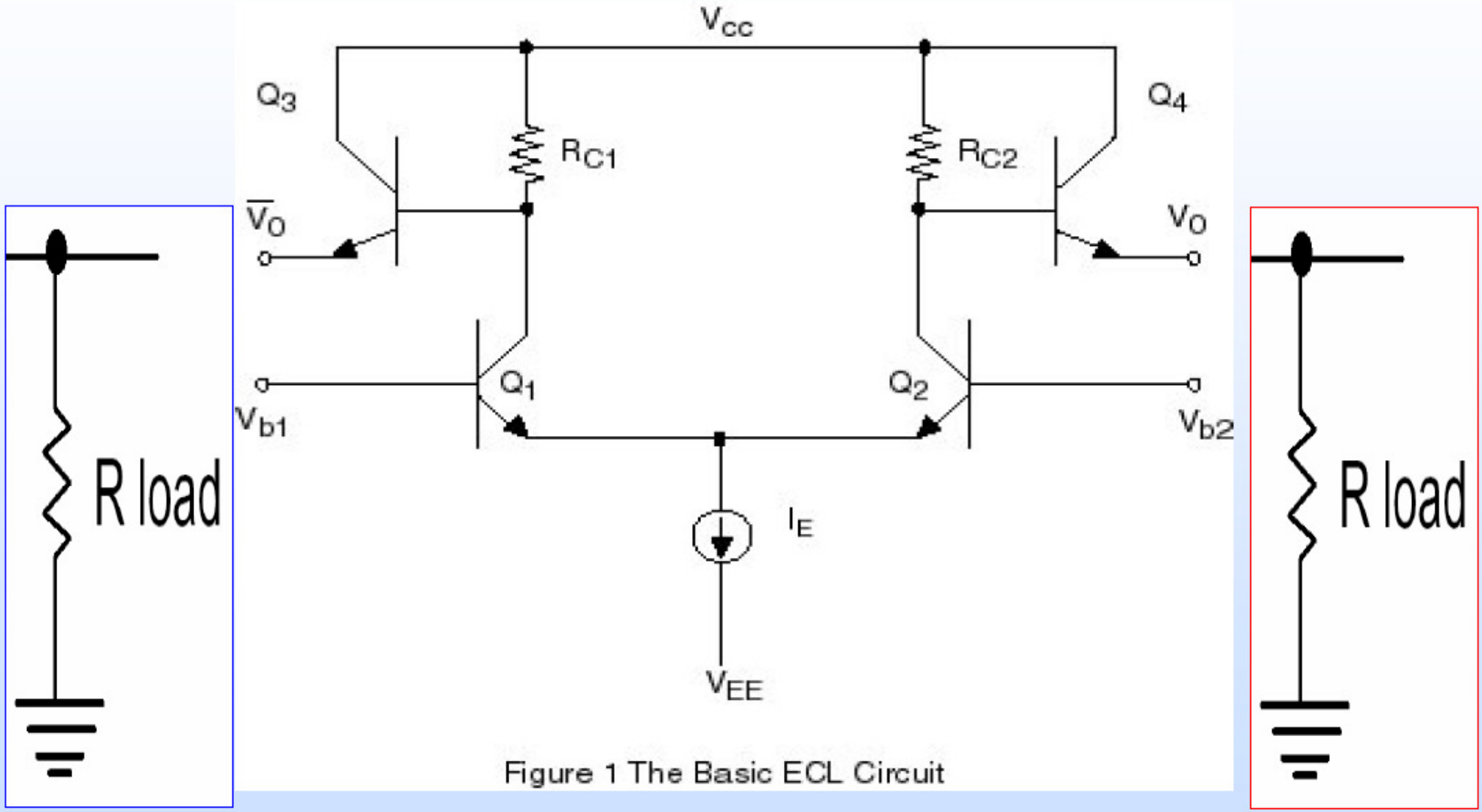

Figure 1 The Basic ECL Circuit

Current-driving mode device

Balanced Device vs Unbalanced Device

- TTL / CMOS OSC → Unbalanced Device
  operating in "saturation region" in TTL logic
- LVPECL / LVDS OSC → Balanced Device
  operating in "active region" in ECL logic
  → switching fast & suitable for "high frequency applications"

Advantage for Balanced Device

- High noise immunity
- Low power consumption
- Low radiated noise
- High integration density

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LVPECL/LVDS Signal Analysis

LVPECL & LVDS signal : DC-signal + AC-signal

- Vc = (½) * (V1 + V2) --- Common Mode Signal
- Vd = V1 – V2 --- Differential Mode Signal

- V1 = Vc + Vd/2
- V2 = Vc - Vd/2

Signal analysis can be implemented easily by math. tool

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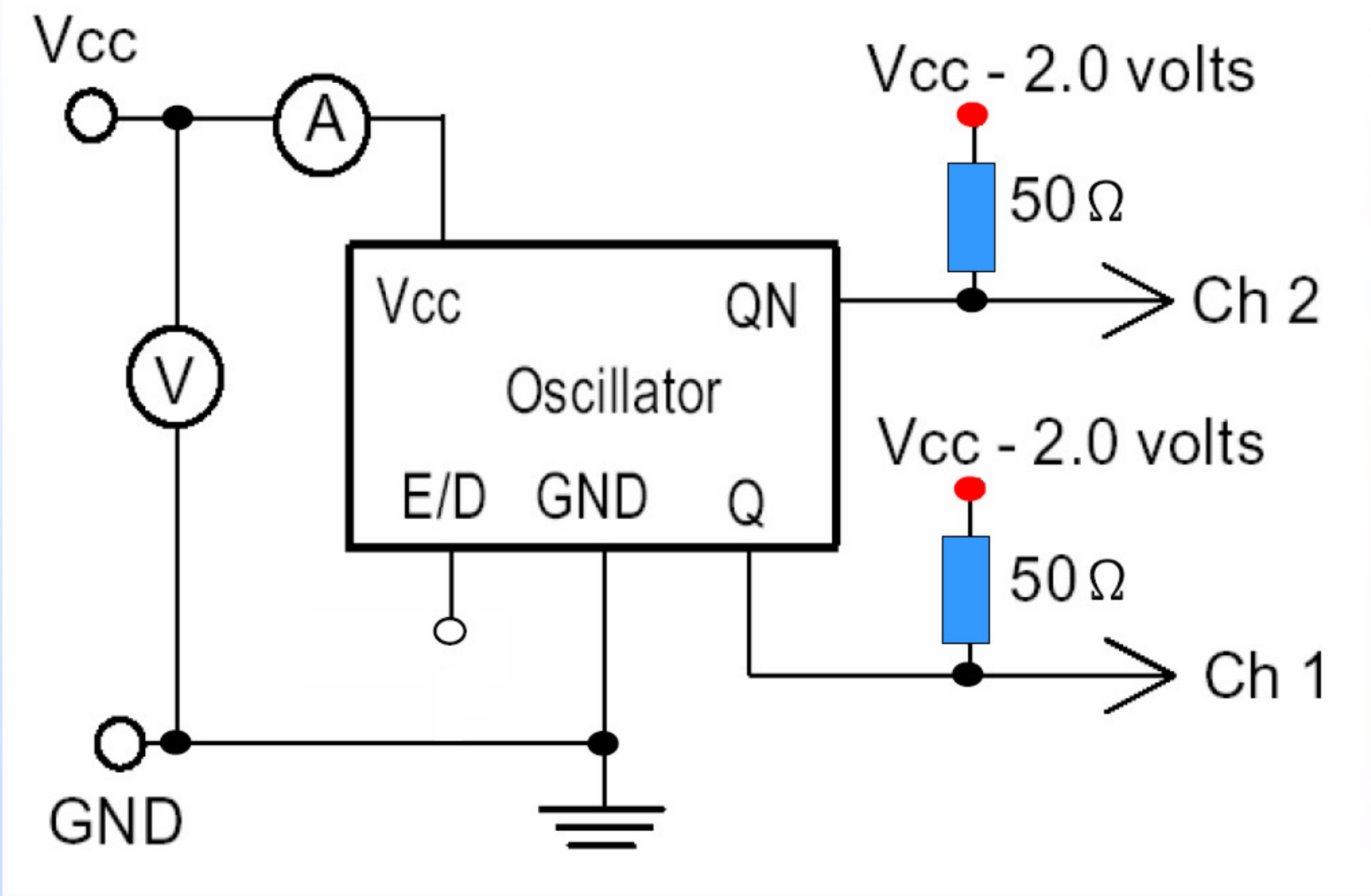
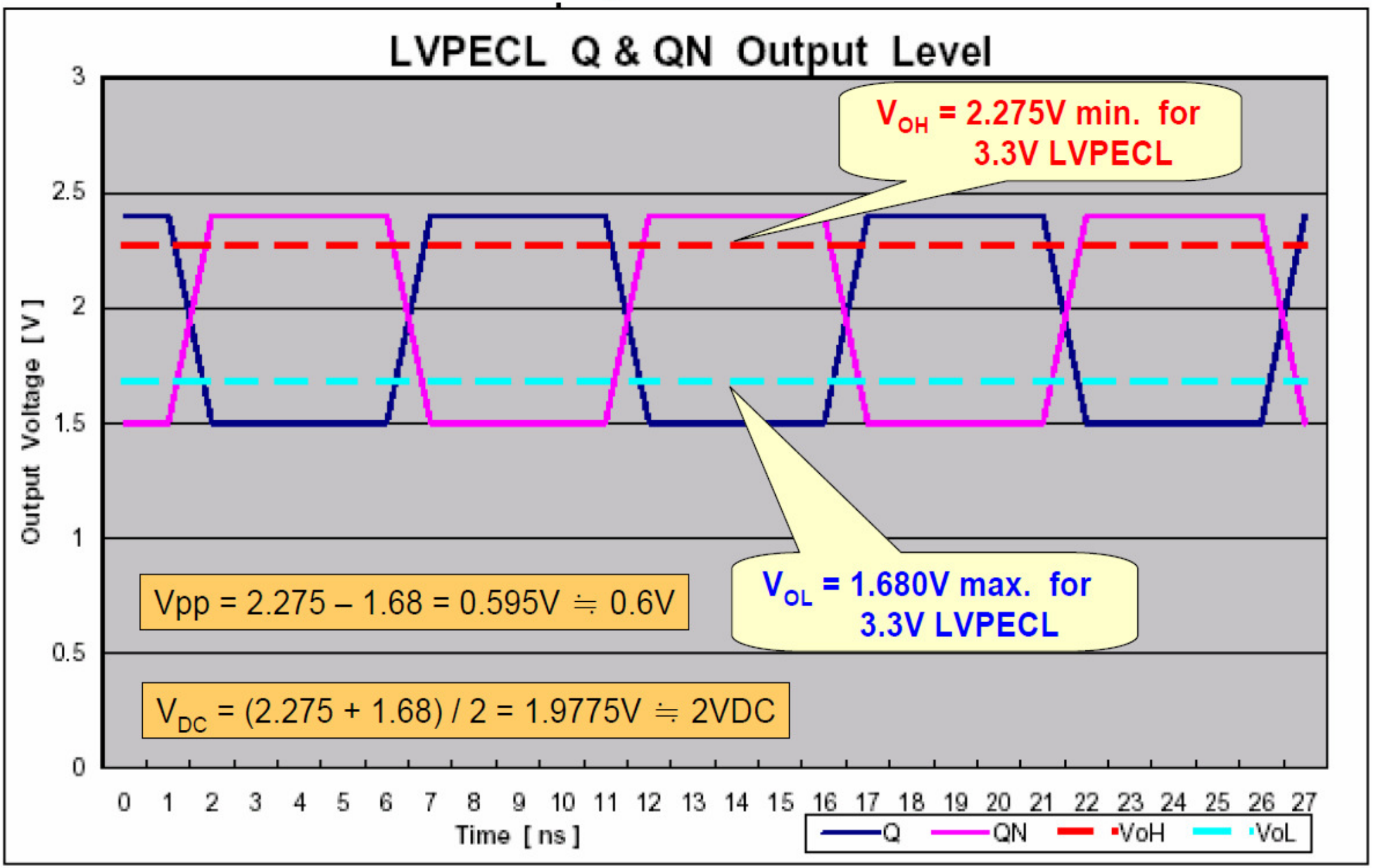
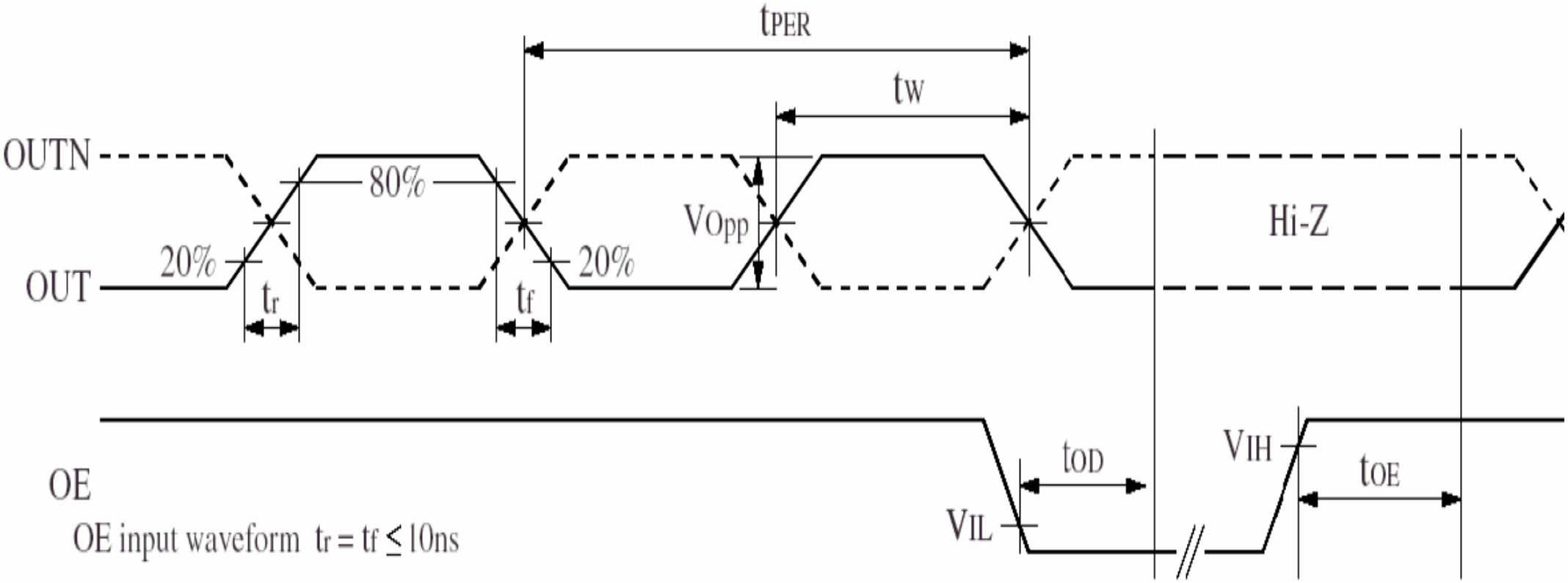
LVPECL Testing circuit



LVPECL Output Level & Waveform



LVPECL output waveform



$DUTY1 = 100t_W/t_{PER}$ (%) @ crossing point

$DUTY2 = 100t_W/t_{PER}$ (%) @ 50% waveform

Timing chart

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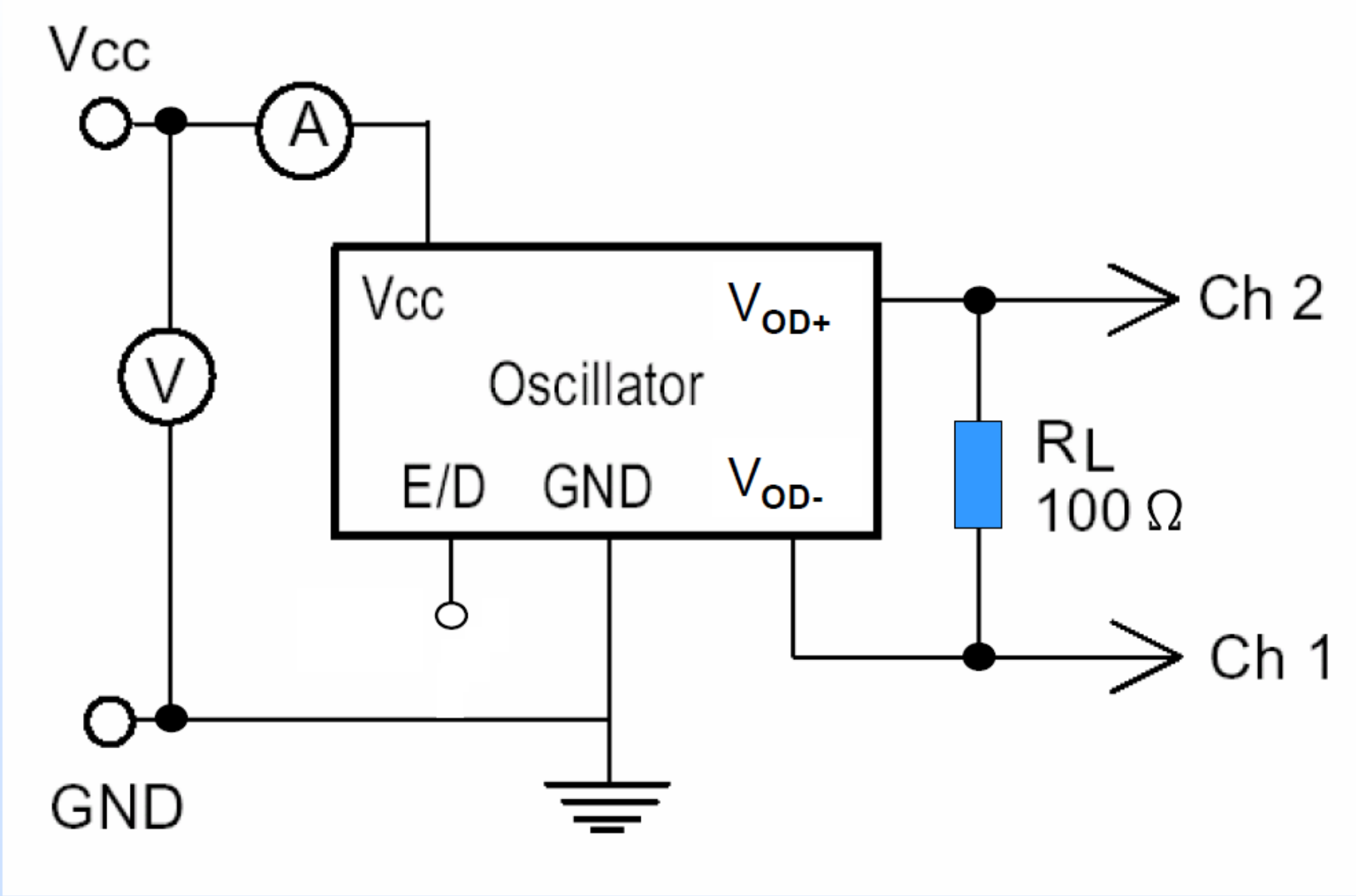
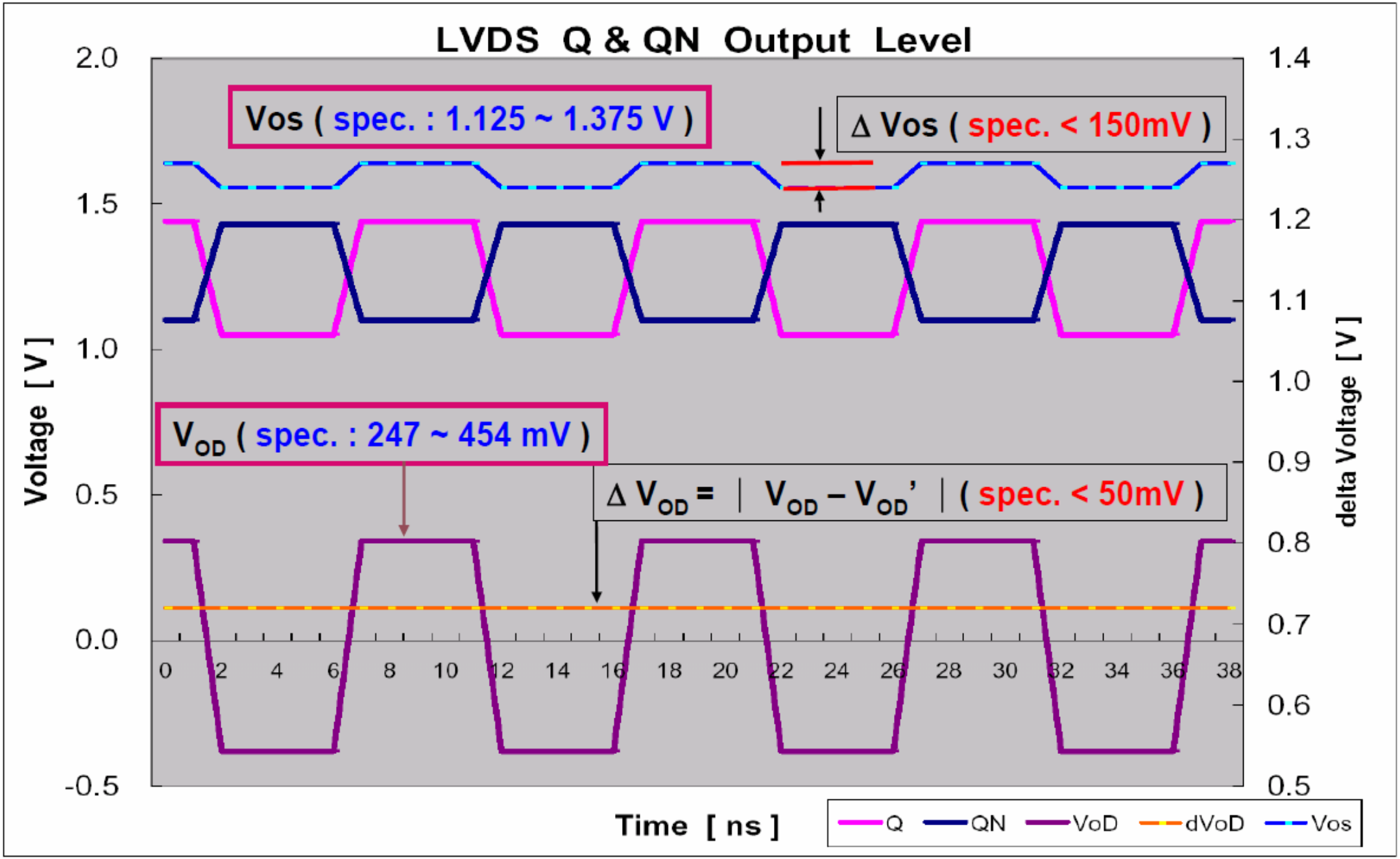
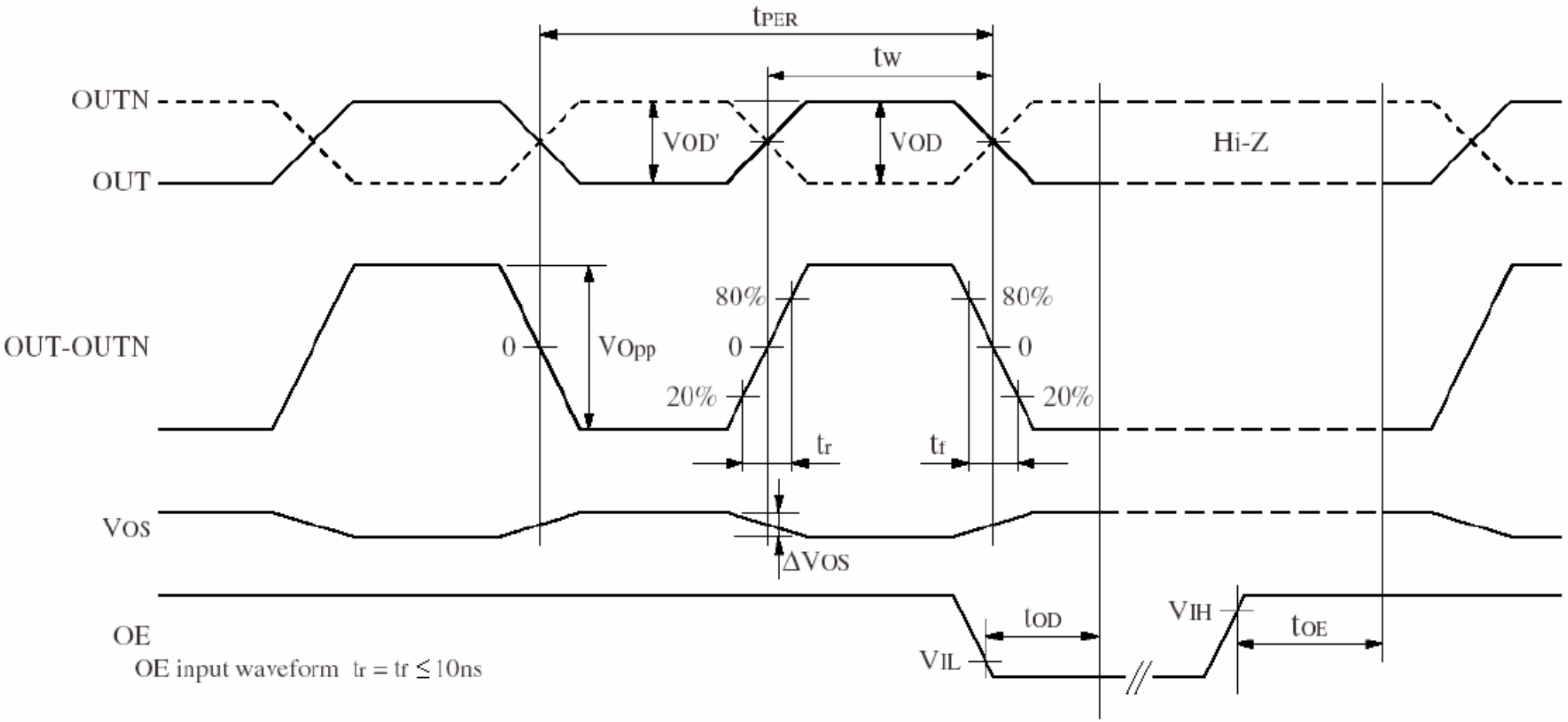
LVDS Testing circuit



LVDS Output Level & Waveform



LVDS output waveform

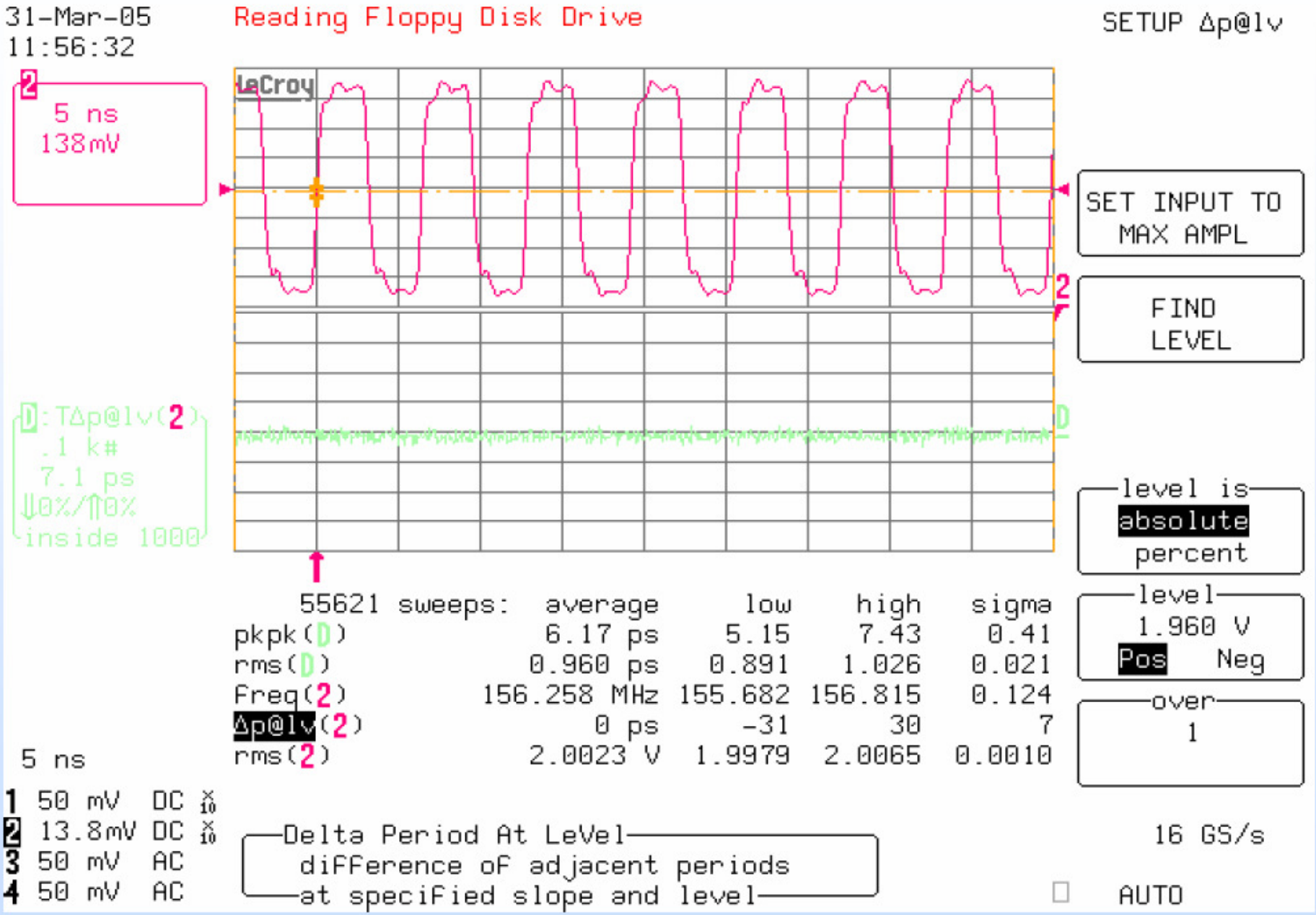


$DUTY = 100t_W/t_{PER}$ (%) @ crossing point

$\Delta V_{OD} = |V_{OD}' - V_{OD}|$

Timing chart

Typical period jitter test data



Period jitter (1 σ) over 50,000 hits less than 1 ps

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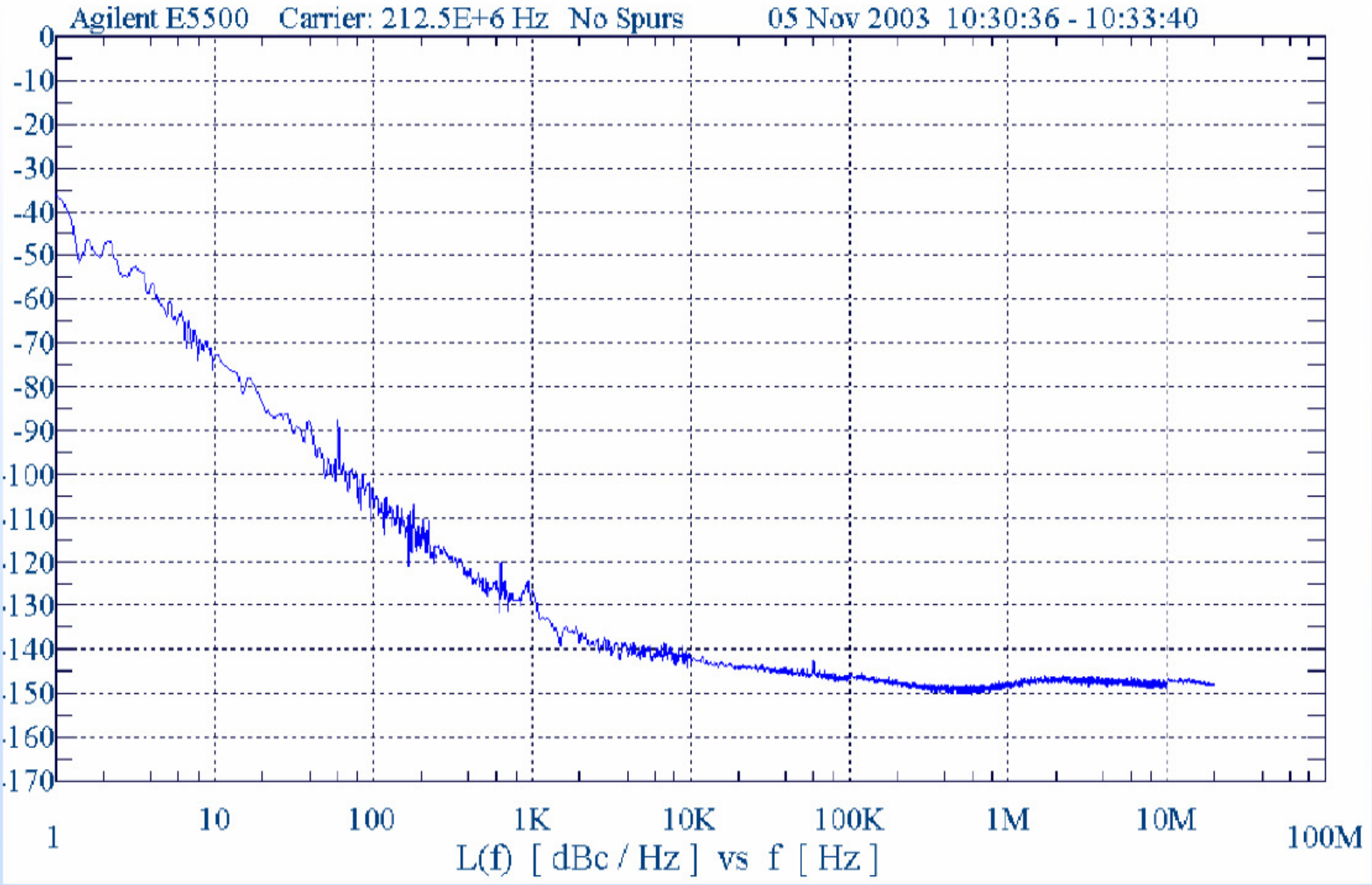
Typical Phase noise test data



High Frequency layout concern - 1

From wavelength point of view

Frequency * wavelength = C $C \sim 3 \times 10^8$ m/sec

$$\lambda = \lambda_o = \frac{c}{f} \approx \frac{3(10^8)\,{}^{m}/_{\sec}}{f\ {}^{c}/_{\sec}} = \frac{30cm}{f_{GHz}} \approx \frac{11.8inch}{f_{GHz}}$$

Frequency	Wavelength
100 MHz	300 cm
1GHz	30 cm
10 GHz	3 cm

High Frequency layout concern - 2

- Assume ε_{eff} is around 3.27 for FR4 PCB
- $\lambda = \lambda_o / \sqrt{\varepsilon_{eff}} = \lambda_o / 1.8$

ex: 200MHz osc

$\lambda = \lambda_o / 1.8 = 150\ cm / 1.8 = 83.3\ cm$

$\lambda / 4 = 83.3\ cm / 4 = 20.8\ cm$

short ←→ open

$10\% * \lambda/4 = 0.1 * 20.8\ cm = 20.8\ mm$

ex: A short via thru a 5mm-length & width 254um & 35um thickness of Cu film

→ $L_{stray} \fallingdotseq 0.85\ nH$ (in 200 ~ 300MHz)

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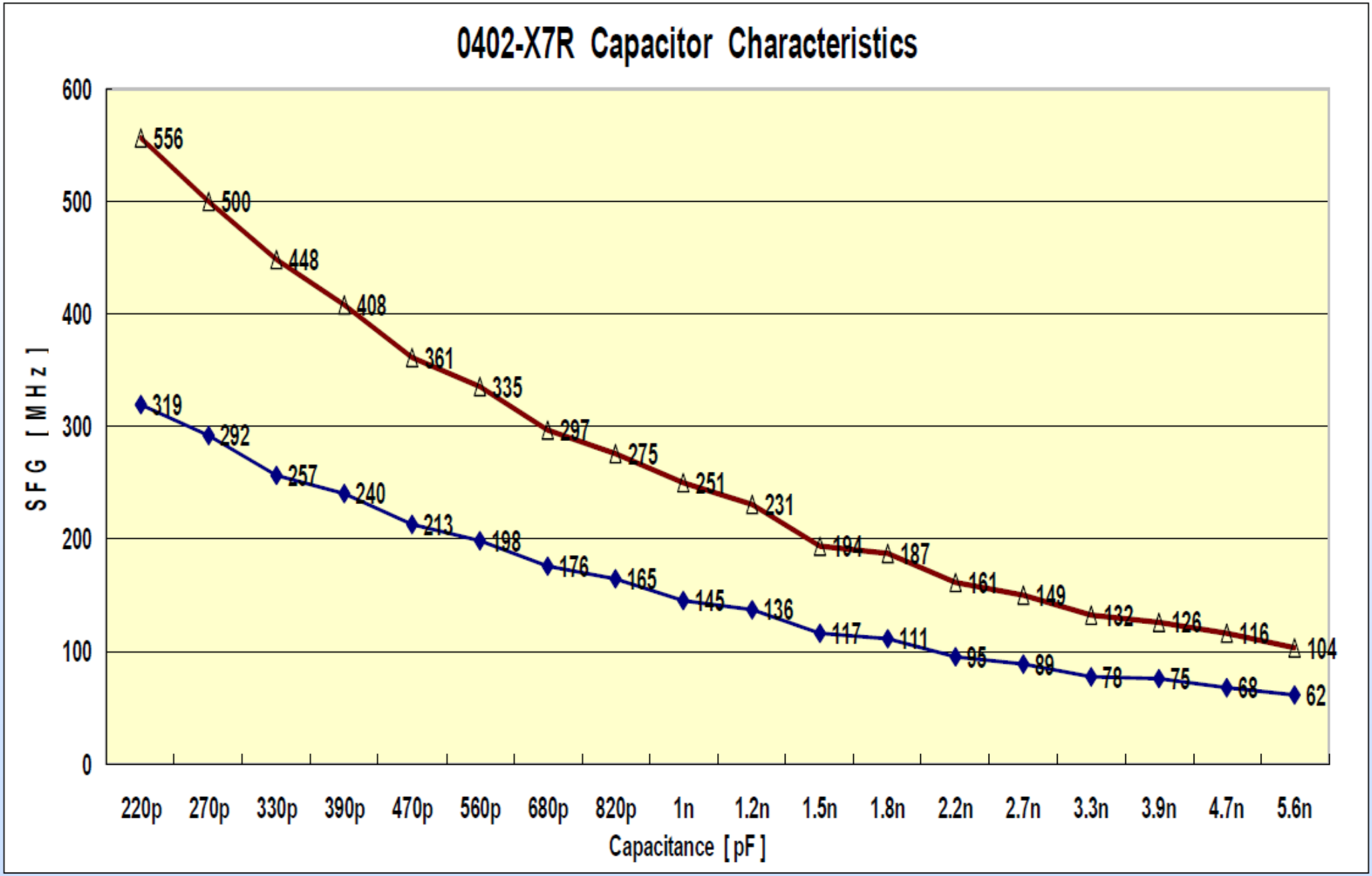
High Frequency layout concern - 3



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AKER Technology Co., Ltd.

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AKER Technology Co., Ltd.

TEL:886-4-2533-5978

FAX:886-4-2533-6011

Email:akertec@aker.com.tw

Web-site: www.aker.com.tw